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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,535	04/15/2004	Tomoaki Shino	251996US2	6547

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EXAMINER	
ARENA, ANDREW OWENS	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,535	SHINO, TOMOAKI	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6 and 8-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6 and 8-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 4, 6, 8, 9, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohsawa (US 6,617,651).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

2. Regarding claim 1, Ohsawa discloses (Fig 4A) a semiconductor device comprising:

a semiconductor substrate (11);

a first insulation layer (12) formed on the semiconductor substrate;

a semiconductor layer (13+16+17) insulated from the semiconductor substrate by the insulation layer;

a source region (16) of a first conduction type (n) and a drain region (17) of the first conduction type (n) formed in the semiconductor layer;

a body region (13) of a second conduction type (p) formed in the semiconductor layer between the source region and the drain region, said body region being capable of storing data by accumulating or releasing electric charge (col 6 ln 60-61);

a second insulation layer (14) formed on the body region;

a word line (15) formed on the second insulation layer and insulated from the body region by the second insulation layer; and

a bit line (BL) electrically connected to the drain region, wherein the area of the body region in contact with the first insulation layer is larger than the area thereof in contact with the second insulation layer (apparent in tapered shape of 13).

3. Regarding claim 4, Ohsawa discloses (Fig 4A) the first insulation layer has a thickness (30-50nm; col 7 ln 57) equal to or less than five times the thickness (10nm; col 7 ln 52) of the second insulation layer.

4. Regarding claim 6, Ohsawa discloses (Fig 4A) the body region has a thickness (25-50nm; col 7 ln 56) equal to or less than three times the thickness (30-50nm; col 7 ln 57) of the first insulation layer.

5. Regarding claim 8, Ohsawa discloses (Fig 32; col 16 ln 40-45) the semiconductor device according to claim 1 further comprising:

a DRAM region including a DRAM having the body region as a part of a memory cell (col 7 ln 1-2);

a peripheral logic circuit formed around the DRAM region .

6. Regarding claim 9, Ohsawa discloses a peripheral logic circuit (col 16 ln 43), inherently disclosing a transistor used in the peripheral logic circuit. Ohsawa does not

limit his transistor to any particular type, therefore the disclosure of Ohsawa encompasses all well-known transistor types, including those which include:

a source region of the first conduction type and a drain region of the first conduction type both formed in the semiconductor layer;

a body region of the second conduction type formed between the source region and the drain region in the semiconductor layer;

a third insulation layer formed on the body region; and

a gate electrode formed on the third insulation layer and insulated from the body region by the third insulation layer, and

wherein the area of the body region in contact with the first insulation layer is approximately equal to the area thereof in contact with the third insulation layer when viewed in a cross section along the gate electrode.

7. Regarding claim 11, Ohsawa discloses (Fig 4A) the area of the body region in contact with the first insulation layer is larger than the area thereof in contact with the second insulation layer (apparent in tapered shape of 13) in a cross section thereof along the word line (the cross section of Fig 4A is viewed along the word line).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa as applied to claims 1 and 11 above, and further in view of Houston (US 6,703,673).

10. Regarding claim 10, Ohsawa differs from the claimed invention only in not disclosing "the impurity concentration at the interface between the semiconductor substrate and the first insulation layer in the DRAM region is higher than the impurity concentration at the interface between the semiconductor substrate and the first insulation layer in the peripheral logic circuit region." Houston teaches varying impurity concentration (col 5 ln 35 – col 6 ln 25) in both the DRAM and periphery logic regions independently (col 5 ln 16-17). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide the device of Ohsawa with a higher channel impurity concentration in the DRAM region than in the periphery logic region, as suggested by Houston; at least to optimize the transistors independently (Houston: col 5 ln 16-17).

11. Regarding claim 12, Ohsawa differs from the claimed invention only in not disclosing "the body region has steps on the side surfaces thereof in a cross section along the word line." Houston teaches LDD implants (col 6 ln 60), which is known to one of ordinary skill in the art to be effected by source/drain extensions. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Ohsawa by providing source/drain extensions (and therefore steps on the side surfaces of the body region), as suggested by Houston; at least to improve transistor performance.

Response to Arguments

12. Applicant's arguments filed 11/04/2005 have been fully considered, but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800